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From: Jacqueline J. Garner
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mark R. Visokay
Serial No.: 10/734,708
Filed: 12/11/2003
Art Unit: 2813
Examiner: Thanhha S. Pham
Docket No.: TI-35227
Conf. No.: 2373
Customer No.: 23494

CERTIFICATION OF FACSIMILE TRANSMISSION

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<input type="checkbox"/> CONTINUATION APP'N	<input checked="" type="checkbox"/> Election
<input type="checkbox"/> DIVISIONAL APP'N	
NAME OF INVENTOR(S): Visokay et al.	
TITLE OF INVENTION: METHOD FOR FABRICATING TRANSISTOR GATE STRUCTURES AND GATE DIELECTRICS THERE OF	
TI FILE NO.: TI-35227	DEPOSIT ACCT. NO.: 20-0668
FAXED: 7/28/2005 DUE: 7/29/2005 ATTY/SECY: JJG/ms	
RECEIPT DATE & SERIAL NO.: Serial No.: 10/734,708 Filing Date: 12/11/2003 Conf. No.: 2373	

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Title: METHOD FOR FABRICATING TRANSISTOR GATE STRUCTURES AND
GATE DIELECTRICS THEREOF

ELECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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(571) 273-8300 on July 28, 2005.	
<i>Marianna Smith</i> Marianna Smith	<i>7-28-05</i> Date

Dear Sir:

With respect to the Restriction Requirement mailed on 06/29/2005, Applicants elect species A-1/B-1. Applicants respectfully submit that claims 1, 2, 10-12, 22-25 and 63-66 are generic. In addition, claims 26-32 are generic to lettered group A and claims 1-25, 33-55, and 63-67 are generic to lettered group B. With the generic claims listed above, claims 3-13, 26, 27, and 33-57 read on the elected species A-1/B-1.

Respectfully submitted,

Jacqueline J. Garner
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